Defect Diagnosis – Reasoning Methodology

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Abstract – Diagnosis has become a crucial technology for early debugging and yield improvement. However, the conventional diagnosis methods are not good at locating the defects that are not precisely expressed only with logical fault models. In this paper, we propose a novel defect diagnosis methodology, which is based on the evaluation of defect behaviors using physical information. We evaluate suspected nodes' behaviors by comparing with the observed responses of ATE. In the evaluation process, we consider "defect activation", which is an estimation of defective nodes' voltage levels using physical information. Using this methodology, we introduce diagnosis examples for open defects in a cell, and for interconnect open defects. Those successful results show effectiveness of the defect diagnosis.

1. Introduction

The progresses of fabrication process and design technology make it difficult to diagnose the causes of failed chips. Many defects such as open, short, or resistive open/short [1], whose defective behaviors are not precisely expressed only with the conventional logical fault models, are increasing. As diagnosis becomes one of crucial technologies for early debugging and yield improvement, an effective diagnosis methodology with high accuracy is strongly required [2].

The conventional diagnosis techniques such as the cause effect or the effect cause analysis [3] usually matches the defects' behaviors to the known logical fault models. Therefore, it is difficult to analyze the defects that are not precisely expressed only with logical fault models [4]. Their target is locating the minimum set of logically equivalent faulty nodes, which may sometimes consist of many nodes (An example of 54 nodes was shown in [5], and 40 nodes was in [6]). However, even a small number of nodes might be difficult to apply physical failure analysis (PFA) because of long wires or many wiring layers in the latest process.

There are some papers [5, 6, 7] that utilize physical information for diagnosis. Sato, et al. [5], diagnosed open defects considering coupling effects with neighboring nodes. The method is specific to open defect. Therefore, it needs to be generalized. Then, this paper addresses a novel generalized diagnosis methodology. We evaluate each suspicious node's behavior by comparing with the observed responses of ATE. In the evaluation, we consider "defect activation". It is an estimation of the defective node's voltage level. The estimation is performed not only at logical level, but also at physical level. Here, the passed vectors don't indicate any non-existence of defects, but it only tells that the logical levels of the defective nodes were the same as the normal nodes'. We examine the suspicious nodes' "defect activations" if they match to the observed responses of ATE. We show two examples of our methodology for an open diagnosis and intra-cell diagnosis using real chips. Although some parts of them were introduced in [5, 15], we introduce them from a more generalized point of view.

The remainder of the paper is organized as follows. Section 2 describes the concept of defect diagnosis. Section 3 discusses "defect activation" and shows some examples. Section 4 introduces some diagnosis using our new methodology and shows its effectiveness. Section 5 concludes the paper.

2. Concept of Defect Diagnosis

In most of the conventional diagnosis, a logical fault (i.e. stuck-at-0 or stuck-at-1) is usually treated as follows:

(1) When a fault doesn't exist, the test will pass.

(2) When a fault exists and logically propagates, the test will fail.

But, this is not always true. For example, an open fault is not observed (i.e. the test will pass.) when the node's voltage is accidentally the same as the correct value. A defect's logical value will be affected with a variety of factors, such as, other nets' logical values, resistance, or capacitance. Therefore, we introduce the concept of "defect activation". It is an estimation of suspicious defect's voltage level. The estimation method differs for each type of defect, and we have to develop methods that simulate its physical defective behavior. We define "activate_1", "activate_0", and "activate_X" as the estimated logical values of the defective node by "defect activation". "Activate_1" means logical 1, and "activate_0" means logical 0. "Activate_X" means that the node's value cannot be decided.

The decision tree of testing result for a vector that propagates a defective node's logical value to primary outputs is shown in Figure 1. When a defect is activated to 1 and the vector's expected value is 1, then, the test will

pass. When expected value is 0, the test will fail. When a defect is activated to X (unknown), the test might pass or fail whatever the expected value is. This seems sometimes almost accidental. This is why conventional diagnosis techniques are not good at treating defects that are not precisely expressed only with logical fault models.

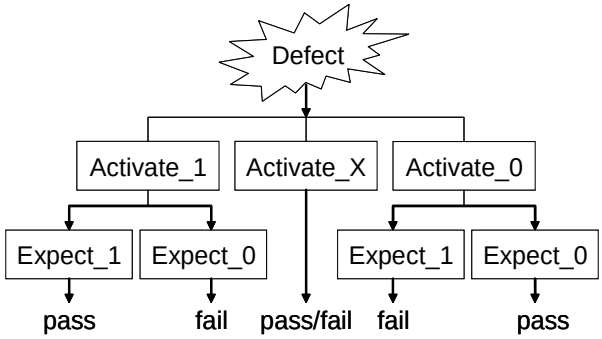

Figure 1 Activation decision tree of defects.

"Defect activation" usually depends on some physical parameters, which are unknown in a fabricated chip. For example, a bridging resistance between two nodes affects defect behavior very much [8]. But, who knows the value? Figure 2 shows the reasoning methodology that we propose.

(1) Firstly, the suspicious nodes are extracted thorough a conventional diagnosis, which may have some mis-predictions [9].

(2) From the ATE responses, extract two kinds of test vector sets. One is a set of vectors in which the suspicious node is observed at high logical level (vectors that detect stuck-at 0 and pass, or detect stuck-at 1 and fail). The other is a set of vectors in which the suspicious node is observed at low logical level (vectors that detect stuck-at 1 and pass, or detect stuck-at 0 and fail).

(3) Next, evaluate each suspicious node's parameterized "defect activation" for test vectors in both sets.

(4) Then, find proper parameters that "defect activation" and the sets in step (2) match well. If there exists proper one, then the node will be one of the located nodes.

(5) Lastly, select the most probable node that has most matching in (4) as the located node.

3 Defect Activations

In this section, we introduce some examples of "defect activations" and discuss parameters that affect them.

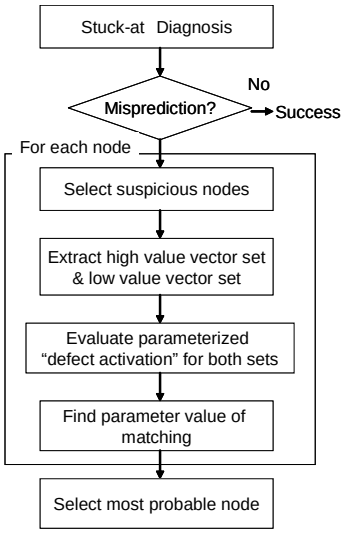

Figure 2 Reasoning methodology.

3.1 Resistive Bridging Defect (Short)

We discuss a bridging defect. When two output nodes V_1 and V_2 of the gates are shorted by resistance Rsh, their voltage will be as follows [8]. The logical value of V_1 is decided comparing to the logical threshold V_{ALT} of the following gate A and that of V_2 is decided comparing to the logical threshold V_{BLT} of the following gate B.

$$V_1 = \left[1 - \frac{R_p}{R_n + R_{sh} + R_p}\right] V_{dd.} \quad (1)$$

$$V_2 = \left[\frac{R_n}{R_n + R_{sh} + R_p}\right] V_{dd.} \quad (2)$$

Where, *Rp* and *Rn* are resistance of PMOS and NMOS transistors respectively when they are activated. In this case, Rsh is a major parameter of "defect activation".

3.2 Open Defect

The behavior of open defects was introduced in several papers [5, 10, 11, 12]. A completely open node's voltage will be affected by the neighboring nodes' voltage. When the neighboring nodes are at high level, the floating node's voltage will be high with coupling effects. When the neighboring nodes are at low level, the floating node's voltage will be low. Then, the floating node's voltage will be expressed as follows [5].

$$V_f = \frac{C_1}{C_0 + C_1} V_{dd} + \frac{Q_0}{C_{gnd}}. \quad (3)$$

Where, V_f is the voltage of the floating node. Q_0 is the initial trapped charge of the floating gate. C_{gnd} is the capacitance between the floating node and the ground rail. C_1 is the sum of the capacitance between the floating node

and the neighboring nodes, which have high voltage values ($\approx V_{dd}$). C_0 is the sum of the capacitance between the floating node and the neighboring nodes, which have low voltage values ($\approx V_{ss}$). It should be noted that they depend on the test pattern *p*. Figure 3 shows a simulation result using 130nm 8-layer process parameters [2]. As the parallel length L (proportional to coupling capacitance) increases, voltage increases, and, at last, is larger than Vt (the following gate's logical threshold voltage). The graph shows that only 20 μm is enough to flip the floating node's logical value. In this case, Q_0 / C_{gnd} is an unknown parameter of "defect activation". C_0 and C_1 are extracted from layout data using a symbolic layout tool or DRC (Design Rule Check) tool. For each test pattern *p*, the logical value of each neighboring node is calculated with logic simulation.

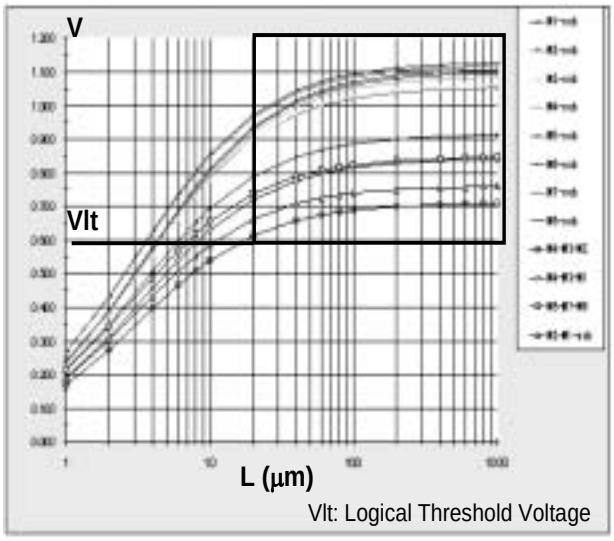

Figure 3 Coupling effect simulations.

3.3 Delay Defect

Delay defect is caused by any kind of resistive defect such as resistive via, resistive wire, or leak transistors. Figure 4 is an example. A defect can be on a stem, or on a branch of the net. It might be close to a sink gate, or close to the source gate. A propagation of defect differs according to its location. When it is on the stem (D_1 on Figure 4, 5), it propagates to all of the branches. When a defect is on a branch (D_2), it doesn't propagate to other branches. Seeing an actual layout topology, the feature is complicated as shown in Figure 4. Figure 5 shows the simulation result of the propagation. When the resistance exists close to the stem, it will influence the delay much. However, when it exists close to the following gate, it will not affect the delay much because of high impedance of input gate (see D_2 and S3 response). In this case, resistance of defect and its location will be a major parameter of "defect activation".

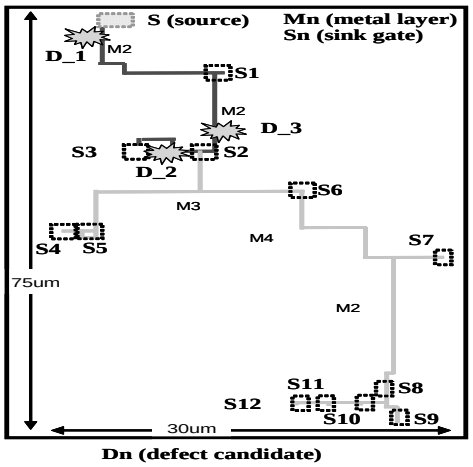

Figure 4 Resistive defect in a net.

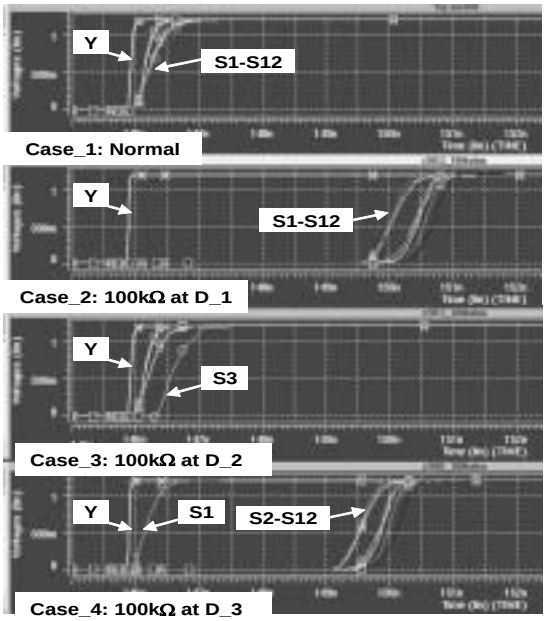

Figure 5 Simulation result of resistive defect.

3.4 Intra-cell Defect

Defects in a gate/cell, such as resistive open/short or resistive leakage, will show complicated aspects [1, 13, 14]. A transistor level simulation is mandatory for accurate evaluation of "defect activation". If we insert a suspicious defect into a transitor circuits as a defective resistance, we can estimate the output values of the defective cell by simulation. In this case, resistance R is an unknown parameter.

4. Experimental Results

4.1 Intra-Cell Diagnosis

We introduce an example of reasoning methodology for intra-cell diagnosis, whose summary was shown in [15]. 4-input AND-OR circuit (Figure 6) was diagnosed. We

extracted the cell's behavior in Table 1 using a cause-effect diagnosis or fault simulation, where shadowed values are false (fail). The cell shows true values and false values for the same input vectors (i.e. It shows an unstable behavior). To evaluate "defect activation", we had an experiment as follows.

(1) Possible fault locations of bridges and opens were extracted from mask data. Bridges were assumed on the area where two metal nodes are close (i.e. within a specified length), and opens were assumed on contact vias.

(2) Resistance was inserted into SPICE net list. We assumed 0 Ω for a bridge, and 100 MΩ for an open via.

(3) Switch level simulation was performed for each vector respectively. For speeding up, a switch level simulator was developed. It treats each transistor as an on/off switch. When a transistor is on, it is regarded as a resistance. When there is no direct current source or there is high resistance, output values were set to "M" (i.e. Hi-Z). When they were in the middle level, they were set to "V" (0.3Vdd – 0.7Vdd interval). After excluding nodes that cause 0/1 level mismatch, the faults were classified into three types of (C_1, C_2, C_3) in Table 2.

(4) Then, switch level simulator was applied sequentially. That means the simulator considers the charge effect of previous vector. Therefore, most of "M"s in step (3) disappeared in Figure 7. (A few increase of 0/1 mismatch were observed because of accuracy program.)

(5) The evaluated values were compared to Table 1. From Table 2, type C_1 and C_2 look less possible to be a real defect because the vectors of C_3 are so stable for No.3 (100 vectors). From Figure 7, VIA (0025) in C_3 has the most matches.

(6) Figure 8 shows the located open via in the circuit, which was actually confirmed by PFA (physical failure analysis). We confirmed the unstableness by SPICE simulation by shifting input vectors' order, which is shown in Figure 9 and 10. We can see that Y is unstable when pre

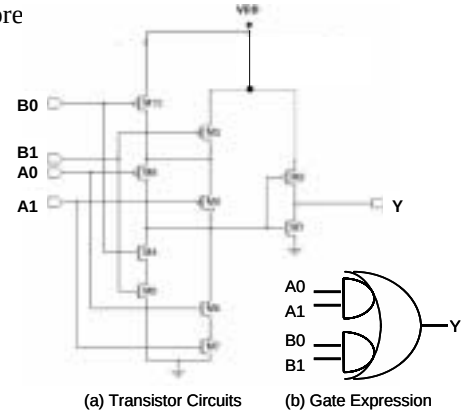

Figure 6 Benchmark circuit.

Table 1 Logical behavior of the defective cell.

A0	A1	B0	B1	Y	# of vectors
0 0	0 0	1 1	1 1	*0*	*16*
				1	1
1 1	0 0	1 1	1 1	*0*	*18*
				1	4
1	1	0	0	1	100
1 1	1 1	1 1	0 0	*0*	*74*
				1	20

Table 2 Defect evaluation (1).

No.	A0	A1	B0	B1	Y	C_1	C_2	C_3
1	0 0	0 0	1 1	1 1	*0* 1	M	V	*M*
2	1 1	0 0	1 1	1 1	*0* 1	M	V	*M*
3	1	1	0	0	1	M	V	*1*
4	1 1	1 1	1 1	0 0	*0* 1	M	V	*M*

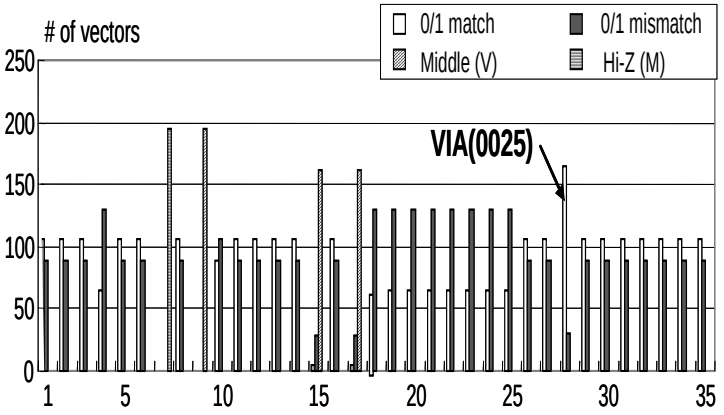

Figure 7 Defect evaluation (2).

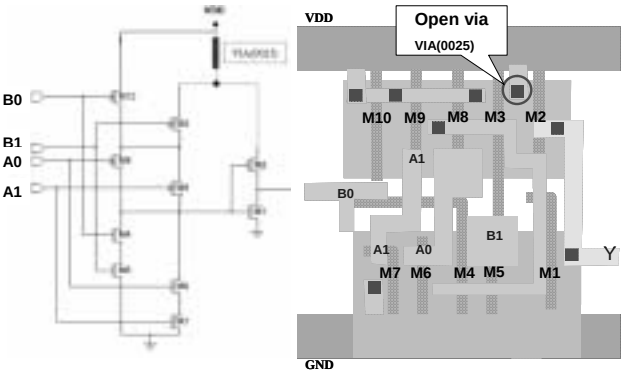

Figure 8 Located open via.

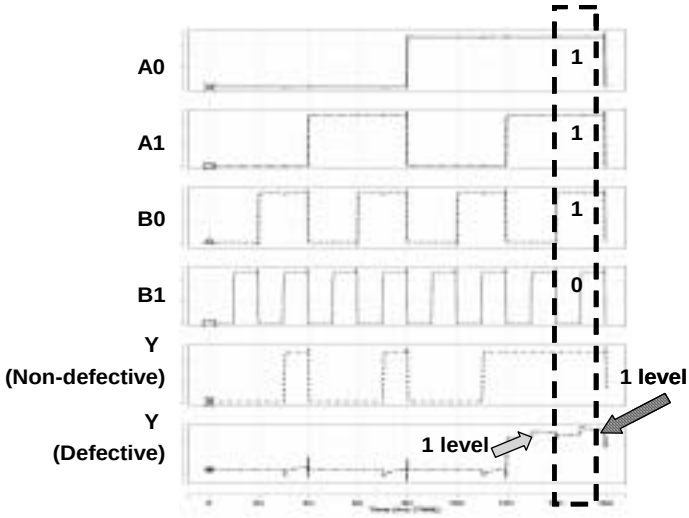

Figure 9 SPICE Simulation (Y is stable when previous level is 1).

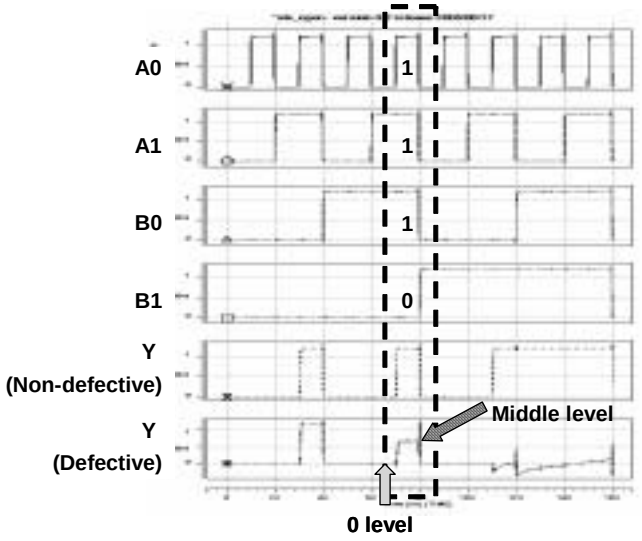

Figure 10 SPICE Simulation (Y is unstable when previous level is 0).

4.2 Open Diagnosis

We will review diagnosis for a completely open defect [5] using our methodology. "Defect activation" is defined according equation (3) in section 3.2. It is evaluated for each via in suspicious nets. A set of vectors, in which the suspicious node is at high voltage level from the ATE's response, is defined as Ω_1. In the same way, Ω_0 is defined. The precise definition of Ω_1 and Ω_0 is as follows (Figure 11).

Ω_0 = {p: a set of test patterns p that should detect the stuck-at-0 fault and should fail} or {p: a set of test patterns p that should detect the stuck-at-1 fault and should pass.}

Ω_1 = {p: a set of test patterns p that should detect the stuck-at-1 fault and should fail} or {p: a set of test patterns p that should detect the stuck-at-0 fault and should fail.}

Using the same notations as in section 3.2, we will define *E (p)* as follows:

$$E = E(p) = \frac{C_1}{C_0 + C_1} = \frac{C_1(p)}{C_0(p) + C_1(p)} \qquad (4)$$

This is the coefficient of equation (3). We also define E (Ω_0) and E (Ω_1) as follows:

E (Ω_0) = [min E (p), max E (p)] for all p in Ω_0 (5)

E (Ω_1) = [min E (p), max E (p)] for all p in Ω_1 (6)

If E (Ω_0) < E (Ω_1) is true for a suspicious via (Figure 11), It is possible that the logical threshold Vlt of the following gate satisfies the following relation.

$\max E(\Omega_0)\times Vdd + Q_0 / C_{gnd} < Vlt < \min E(\Omega_1)\times Vdd + Q_0 / C_{gnd}$.

Then,

$Vlt - \min E(\Omega_1)\times Vdd < Q_0 / C_{gnd} < Vlt - \max E(\Omega_0)\times Vdd$. (7)

This shows the possible existence of proper parameter for "Activation conditions" that was discussed in section 3.2. This is a prerequisite requirement for open defect, and is not a sufficient condition. However, our following experiments show that it is practical method.

Table 3 shows examples of the method, which were of 130nm process technologies. Sample#1 is the one introduced in [5]. Sample #1, 2, 5, 7 were successfully diagnosed using our methodology. In each sample, the number of nets, the number of vias, and the total length was reduced drastically. A stacked via was located in sample #5. Figure 12 shows the evaluation of E (Ω_0) and E (Ω_1) for each via in a suspicious net that was located by the conventional stuck-at-based diagnosis. The interval from via #14 to via #53 satisfies the condition (7). A segment open was found between via #47 and #48 by PFA. The total CPU time of reasoning was 5h 32min.

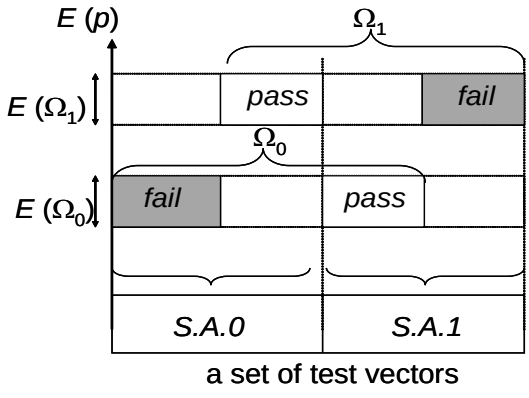

Figure 11 Comparison of ATE results and activation result.

Table 3 Open diagnosis experiments

Sample No.	Stuck-at diagnosis			Reasoning			Result
	# of net	# of via	Total length (μm)	# of net	# of via	Total length (μm)	
1	54			1	1	0	Open[7]
2	3	110	4,000	1	40	1,090	open
3	2	15	600	-	-	-	
4	2	54	1,050	-	-	-	
5	3	51	2,430	1	5	0.8	open
6	1	5	70	1	40	-	bridge
7	3	32	414	1	15	297	open
8	5	105	808	-	-	-	

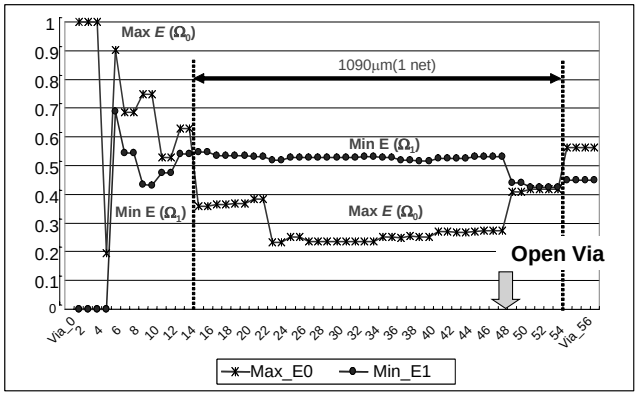

Figure 12 Via estimation of sample 2.

5. Conclusion

We introduced a reasoning methodology for defect diagnosis that aims especially at the defects that are not precisely expressed only with logical fault models. We addressed "Defect Activation", which estimate defective node's voltage using physical information, and showed some examples. Estimating physical behavior of defects often requires some parameters that are unknown to us. We showed our methodology is usable in such case. We also showed experimental results of an intra-cell diagnosis, and an open diagnosis. These results show the effectiveness of our defect diagnosis methodology.

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