Voltage-based fault path tracing by transistor operating point analysis

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Article history:
Received 3 July 2008

Abstract

A novel diagnosis technology based on transistor operating point analysis is presented. This technology is the way to detect penetration current net result from fault, replace the net with impedance net, calculate voltage value of each node of the impedance net by OHM's law, and then sequentially trace the fault logic propagation. The impedance is determined by using transistor dimension and its operating point managed by gate voltage. The proposed method makes it possible to detect not only signal propagation of each gate in order of time, but oscillation phenomenon brought by feedback fault.

1. Introduction

Since an advanced LSI with large-scaled and multi-metal layers makes it difficult to detect fault portions by only physical analysis tool, fault diagnosis technology has been developed to assist it. Until now, diagnosis has aimed to detect irregular portions on connection line between cells. Recent LSI has been, however, converting to design surrounding, which brings the strictness of design rule and the increment of 500 transistors or more in cell circuit, and hence transistor level diagnosis taking notice of intra-cell circuit has been requested. SPICE (simulation program with integrated circuit emphasis) being one of representative transistor level analysis tools is wildly used to evaluate precisely circuit behavior. SPICE is, however, non-effective tool for a diagnosis expecting simple operation and short turn around time (TAT).

To clean up the above problems, a effective diagnosis technology has been developed which is substituted for SPICE [1,2]. A simplified diagnosis procedure is shown in Fig. 1. The diagnosis procedure starting from fault circuit area, which has un-adjusted relation between IN and OUT logic detected by publicly known technology, takes candidate fault portions out of layout data. Each fault is embedded on the circuit and the relation between IN and OUT logic is studied by logic simulation based on voltage. The portion bringing the logic according with real fault logic is determined as high reliable fault portion. After that, physical analysis of each reliable portion is started.

The purpose of this paper is to show the voltage-based diagnosis method to trace fault path by transistor operating analysis. The paper consists of five sections. In Section 2, the way of candidate faults detection using layout data is presented. Section 3 introduces a concept of the proposed diagnosis technology, detection procedure and device for fault path tracing. In Section 4, a couple of diagnosis result using the proposed technology are reviewed. Section 5 concludes the paper.

2. Candidate faults detection by layout data

The way of candidate faults detection using layout data is presented. The detection of candidate fault portions embedded on the circuit is described. Two kinds of bridging faults are adjoining and crossed lines. These portions are easy to detect by layout data: DEF, LEF and Cell design data. For the selection of more reliable fault portions, the priority ranking is applied by using the size of the area that laps by expanding the line width (see Fig. 2).

3. Diagnosis concept

In this session, after a concept of the diagnosis procedure is presented, the detection way of impedance value being basic to this technology is described. One data for the way is transistor dimension, and other is its operating point. Next, the detection procedure is presented, and finally device for fault path tracing is introduced.

3.1. Diagnosis concept

The diagnosis technology being assist tool of physical analysis is requested with easy operation and short TAT. One of simple technologies is switching level simulation (SLS). SLS has been wildly used to evaluate the CMOS logic which treats each transistor as ON/OFF switching path. One of SLS applications is switching path modeling treated as stuck-at fault [3,4]. Voltage rather than stuck-at fault value is, however, beneficial data for precise fault diagnosis, and hence a novel way combined SLS with voltage analysis on transistor level has been developed.

The concept of this way is that transistor discerned as ON-switching path by SLS is replaced with impedance, and the circuit net composed of the transistors is replaced with impedance net,
The transistor operating point managed by gate voltage \( (V_{G}) \) affects impedance. When the power supply voltage \( (V_{DD}) \) is applied to the gate terminal, the operating point of N channel transistor (NchTr) and P channel transistor (PchTr) lies in non-saturation and cut-off area respectively, and the inverse of the gradient value between the NchTr’s operating point and the origin \((\Delta V_{DS}/\Delta I_{DS})\) is assigned as NchTr’s normal impedance value. When the ground (GND), the operating point of NchTr and PchTr lies in cut-off and non-saturation area respectively, and the inverse of the gradient value between the PchTr’s operating point and the origin \((\Delta V_{DS}/\Delta I_{DS})\) is assigned as PchTr’s normal impedance value. When the middle voltage out of \( V_{DD} \) or GND is applied to the gate terminal, the operating points of them are seated out of cut-off area and the impedance is several times larger than normal one.

The detection of the impedance is explained using Inverter gate. Fig. 3 shows the voltage transfer characteristics (VTC) of Inverter gate (see Fig. 3a) and the drain current \((I_{DS})\) versus drain voltage \((V_{DS})\) characteristics of NchTr and PchTr (see Fig. 3b), composing the Inverter gate. The coordinate system of PchTr is displayed according with NchTr. The area within \( |dV_{OUT}/dV_{IN}| > 1 \) decided by VTC curve is defined as middle domain (MD) with large impedance. When \( V_{IN} \), being input-voltage \((V_{IN})\) shown in Fig. 3a, is applied to INPUT terminal, PchTr operating point and NchTr are settled at point A shown in Fig. 3b. As a result, the PchTr’s impedance/NchTr are calculated as the inverse of gradient value connecting point A and the origin \((V_{DD}/0)\) respectively, and the ratio of these values to the normal impedance value is computed.

For effective diagnosis, the table of impedance ratio of MD to normal domain is prepared on ahead. Fig. 4 shows the relation between VTC and impedance ratio, computed by Inverter gate designed with 0.35 \( \mu \)m rule. The area within 35% for \( V_{DD} \) to 65% is defined as MD. The impedance ratio in the MD is classified five steps (2 times, 3, 4, 5 and 6). The table shown in Fig. 4 denotes that PchTr/NchTr’s impedance ratio in the range from 35% of \( V_{DD} \) to 42% are 2/6, 42% to 48% are 3/5, 48% to 52% are 4/4, 52% to 58% are 5/3, and 58% to 65% are 6/2 respectively.

At Appendix, an example of impedance calculation is introduced.

### 3.2. Detection procedure

An impedance detection procedure depending on bridge is shown in Fig. 5. The circuit with miss function by bridge brings generally penetration current net. First, transistor with the gate terminal connected to the fault line is treated as ON-state, and transistor, and the ratio of \( L \) to \( W \) of the standard transistor is detected as normalized value. The impedance ratio of the various transistor is calculated as the ratio of \( L/W \) value to the normalized value.

#### 3.1.2. Transistor operating point

Candidate fault portions (by layout data)

Fault area (by publicly known tech.,)

Logic simulation (by voltage based)

High reliable fault portions

Physical analysis

For example of impedance detection, MN3, MN5 and MP5 are used at Appendix.
all transistors on the penetration current net are replaced with ON-
switching path by SLS, following which impedance value is added

to the transistors. At the addition of impedance, the simulation is
repeated to draw out the optimized relation between gate voltage
and impedance. Next, the switching path net is replaced with

impedance net. After that, voltage of each node on the impedance
net is computed by OHM’s law.

3.2.1. Device for fault path tracing [5]

For fault path tracing, a virtual terminal (ViT) is prepared at output
point which PchTr aggregate and NchTr one join. Each gate,
composed of these transistors, is treated as one event unit of which
operation time is defined as a normalized value “1”, and hence the
logic propagation time is obtained in the total number of event that
the logic passes through.

4. Evaluation

In this session, the proposed diagnosis technology is evaluated.
One is diagnosis precision by the comparison with SPICE, and other
is fault path tracing bringing oscillation phenomenon.

4.1. Diagnosis precision compared with SPICE

Diagnosis accuracy was evaluated by using faulty full adder (FA)
circuit with 3 inputs (A, B, C) and 2 outputs (COUT, SOUT). Table 2
shows logic table denoting normal logic and abnormal one. Abnor-
mal logic in COUT was detected in 3 of 8 patterns which were com-

bination with 3 input logic. SOUT was normal state. The 44 pieces

candidate fault patterns were detected by layout data, shown in
Fig. 6. White rectangle/cycle patterns indicate candidate adjoining/
crossed line portions. Note that line pairs between power supply
voltage (VDD or GND) and signal are not illustrated. Each candidate
fault portions was embedded in the FA circuit. Relation between IN
and OUT logic was detected by the simulation shown in the follow-
ning procedure, and the fault portions were narrowed down, accord-

ing with real fault logic. The diagnosis judged adjoining pair
between Inverter (Inv) output line and 2-INPUT NAND (2inN) out-
put line as fault portion. Fig. 7 shows FA circuit with the detected
bridge fault. Fig. 7a indicates gate level circuit image and Fig. 7b

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>COUT</th>
<th>SOUT</th>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Normal output</td>
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<td>0</td>
<td>1</td>
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Abnormal state | Normal state

Fig. 5. Diagnosis procedure for bridge.

![VTC and VDS - ID curve of inverter gate.](image1)

![Relation between VTC and impedance ratio table.](image2)

![Diagnosis procedure for bridge.](image3)
shows transistor level circuit of the detected fault area. The logic function of In1 and In2, being INPUT terminal, are indicated as NO-T(A + B) and C, respectively.

When input-logic (1, 1) is applied to input-terminal (In1, In2), normal circuit brings ON-state to N1, N3 and P2, and output (Out) does output “H” level. The circuit with the bridge, however, forms a penetration current net connecting from VDD to GND through P2 and N1, and the voltage of the line connected to P2 and N2 gate terminal changes from GND to middle voltage out of VDD or GND, following which a penetration current net pass through P2, N2 and N3 is newly formed. The transistors on the penetration current net are set down as ON-state, and the penetration current net is replaced with ON-switching path by SLS. These transistors on the path net are replaced with impedance net with optimized value by impedance detection way. After that voltage of each node on the net is computed by OHM’s law, the output voltage is detected as 0.23 VDD according to Eq. (1). Note that nP2 and nN2 mean additional ratio for a standard value, and nP1, nN1 and nN3 with normal Vc are approximately “1”.

\[
V_{\text{OUT}} = \left( \left( 1 + \frac{n_{N2}}{1} \right)^{-1} \left( \left( 1 + \frac{n_{N2}}{1} \right)^{-1} + n_{P2} \right) \right) \cdot V_{\text{DD}} = 0.23 \cdot V_{\text{DD}}
\]

\[
V_{\text{OUT}} = \left( \left( \frac{n_{N2}}{n_{P2}} + 1 \right)^{-1} \left( \left( \frac{n_{N2}}{n_{P2}} + 1 \right)^{-1} + 1 \right) \right) \cdot V_{\text{DD}} = 0.23 \cdot V_{\text{DD}}
\]

\[
V_{\text{OUT}} = \frac{1}{1 + \left( \frac{n_{N2}}{n_{P2}} + 1 \right)^{-1}} \cdot V_{\text{DD}} = 0.23 \cdot V_{\text{DD}}
\]

\[
V_{\text{OUT}} = \frac{1}{1 + \left( \frac{1}{1 + \frac{n_{N2}}{1}} + 1 \right)^{-1} + n_{P2}} \cdot V_{\text{DD}} = 0.23 \cdot V_{\text{DD}}
\]

\[
V_{\text{OUT}} = \frac{1}{1 + \frac{n_{N2}}{1}} \cdot V_{\text{DD}} = 0.23 \cdot V_{\text{DD}}
\]
When input-logic (0,1), the similar way to the above diagnosis detects output value with 0.82 VDD (see Eq.(2)).

SPICE indicates that input-logic (1,1) outputs 0.25 VDD and input-logic (0,1) outputs 0.83 VDD. Both result denoted same output-voltage. Fig. 8 shows the characteristics of logic relation between $V_{IN}$ (In1, In2) and $V_{OUT}$ (Out), and the comparison of diagnosis accuracy between this technology and SPICE result with or without bridge. Operation time of this way was 1/100 times of SPICE by using SUN_ULTRA_60.

4.2. Fault path tracing with oscillation phenomenon

Fault path tracing was evaluated by using simple circuit with four steps sequential Inverter gate (Inv1-Inv2-Inv3-Inv4) shown in Fig. 9. Inv4 is composed of parallel connection inverter gates and bridging fault is formed between Inv1 output line and Inv4 one. Note that all of the transistors composing Inverter gate are standard dimension type.
When “L” level is applied to Input (IN), “H” level is outputted at the Inv1 output terminal and “L” level is at Inv4, and the logic collision through the feedback loop between Inv1 output and Inv4 is generated, following which a penetration current net is brought by the logic collision phenomenon, and the net is treated as new event unit.

The logic collision which brings penetration current makes OFF-state of P4 and P5 and ON-state of P1, N4 & N5, and ON-switching path net is formed from VDD to GND through P1, N4 and N5 by SLS (see Fig. 10a).

The ON-switching path net is replaced to impedance net, and voltage of each node is calculated, and hence the value of ratio is calculated as “1/3 · VDD” according in Eq. (3). Note that nP1, nN4 and nN5 mean additional ratio for a standard value.

This value is judged as “L” because of outside of MD. The logic is propagated through Inv2 and Inv3, and “H” level is outputted at Inv4 terminal. Inv1 output logic is “H”, and hence P1, P4 and P5 are ON-state, and N4 and N5 are OFF-state. This state does not bring logic collision and W2 value is kept to “H” level (see Fig. 10b). The above operation is repeated and the oscillation phenomenon is generated, shown in Fig. 11. The logic propagation time is obtained in the total number of event which logic passes through.

The simulation result of Input logic “L” is shown in Fig. 12. Time/pin/value, shown in Fig. 12, means event number/transistor drain or line name/logic value (1, 0, H, L, Z) respectively. Time 1 to 3 shows logic initializing state. From time 4, diagnosis is started. At time 5 and 17, the logic collision is indicated, and at time 11 shows normal state. The oscillation phenomenon is repeated to each 3 event-times. Note that “W” being line name without operation time, does not be counted as event time.

By the similar diagnosis method, an oscillation phenomenon of the circuit applying input “H” is detected. In the oscillation, logic repeats between 2/3 · VDD and GND.

5. Conclusion

For fault path tracing, diagnosis technology combined with switching level simulation has been developed. The technology is the way to detect penetration current net result from fault, replace the net with impedance net, and calculate voltage value of each node of the impedance net. The segmentation of impedance value that was calculated by transistor operating point managed by gate voltage improved the fault diagnosis precision. The virtual terminal (VIT), that was prepared at output point which PchTr aggregate and NchTr one join, made it possible to trace the fault path propagation. The comparison of this way with SPICE indicated an approximately same diagnosis result. Operation time of this way was 1/100 times of SPICE using SUN_ULTRA_60. The detected doubtful portions are quickly applied to physical analysis.

Acknowledgement

I would like to thank the design crew at ASTRON Corp. in Japan for discussion and software development.

Appendix

An example of impedance detection is presented using cell design data shown in Table 1. MN5 (NchTr) with 1/W = 0.1 μ/1.20 μ and MP5 (PchTr) with 1/W = 0.1 μ/1.92 μ composing Inverter gate are selected as standard transistor. Considering MN3 (NchTr) with 1/W = 0.1 μ/0.45 μ, the L/W value ratio of MN3 to standard transistor MN5 is calculated as 2.67 (see Eq. (4)).

\[
\text{MN3} (L/W = 0.1 \mu/m/0.45 \mu) / \text{MN5} (L/W = 0.1 \mu/m/1.20 \mu) = 2.67
\]

When 0.46 VDD voltage is applied to MN3 gate terminal (VIN = NchTr’s VG), the impedance ratio of the MN3 operating domain to normal operating domain is detected as 5 times (see Fig. 4). The impedance is, as a result, calculated as 13.33, being the multiplication of the ratio of L/W value and the ratio of impedance value led by operating point (see Eq. (5)).

\[
2.67 \times \text{additional ratio}(5) = 13.33
\]

References