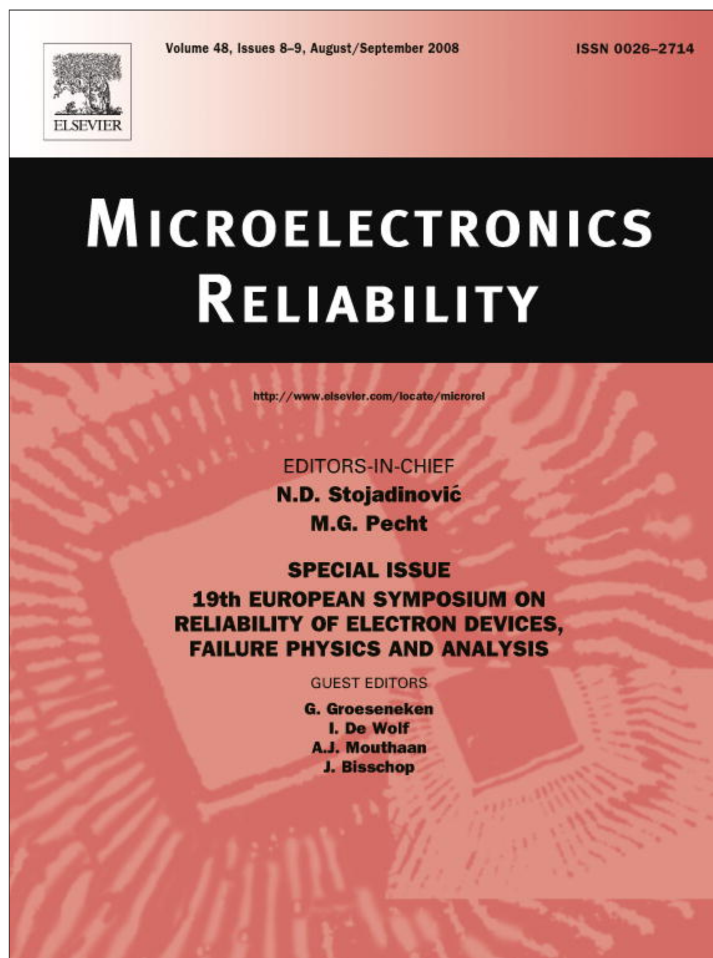
Provided for non-commercial research and education use.
Not for reproduction, distribution or commercial use.



This article appeared in a journal published by Elsevier. The attached copy is furnished to the author for internal non-commercial research and education use, including for instruction at the authors institution and sharing with colleagues.

Other uses, including reproduction and distribution, or selling or licensing copies, or posting to personal, institutional or third party websites are prohibited.

In most cases authors are permitted to post their version of the article (e.g. in Word or Tex form) to their personal website or institutional repository. Authors requiring further information regarding Elsevier's archiving and manuscript policies are encouraged to visit:

http://www.elsevier.com/copyright

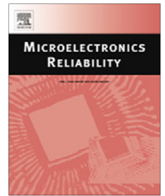
Author's personal copy

Microelectronics Reliability 48 (2008) 1533–1538

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Voltage-based fault path tracing by transistor operating point analysis

Masaru Sanada *

Department of Electronic and Photonic Systems Engineering, Kochi University of Technology, Kami-shi, Tosayanada-machi, Kochi 782-8502, Japan

ARTICLE INFO

Article history:
Received 3 July 2008

ABSTRACT

A novel diagnosis technology based on transistor operating point analysis is presented. This technology is the way to detect penetration current net result from fault, replace the net with impedance net, calculate voltage value of each node of the impedance net by OHM's low, and then sequentially trace the fault logic propagation. The impedance is determined by using transistor dimension and its operating point managed by gate voltage. The proposed method makes it possible to detect not only signal propagation of each gate in order of time, but oscillation phenomenon brought by feedback fault.

© 2008 Elsevier Ltd. All rights reserved.

1. Introduction

Since an advanced LSI with large-scaled and multi-metal layers makes it difficult to detect fault portions by only physical analysis tool, fault diagnosis technology has been developed to assist it. Until now, diagnosis has aimed to detect irregular portions on connection line between cells. Recent LSI has been, however, converting to design surrounding, which brings the strictness of design rule and the increment of 500 transistors or more in cell circuit, and hence transistor level diagnosis taking notice of intra-cell circuit has been requested. SPICE (simulation program with integrated circuit emphasis) being one of representative transistor level analysis tools is wildly used to evaluate precisely circuit behavior. SPICE is, however, non-effective tool for a diagnosis expecting simple operation and short turn around time (TAT).

To clean up the above problems, a effective diagnosis technology has been developed which is substituted for SPICE [1,2]. A simplified diagnosis procedure is shown in Fig. 1. The diagnosis procedure starting from fault circuit area, which has un-adjusted relation between IN and OUT logic detected by publicly known technology, takes candidate fault portions out of layout data. Each fault is embedded on the circuit and the relation between IN and OUT logic is studied by logic simulation based on voltage. The portion bringing the logic according with real fault logic is determined as high reliable fault portion. After that, physical analysis of each reliable portion is started.

The purpose of this paper is to show the voltage-based diagnosis method to trace fault path by transistor operating analysis. The paper consists of five sections. In Section 2, the way of candidate faults detection using layout data is presented. Section 3 introduces a concept of the proposed diagnosis technology, detection procedure and device for fault path tracing. In Section 4, a couple of diagnosis result using the proposed technology are reviewed. Section 5 concludes the paper.

2. Candidate faults detection by layout data

The way of candidate faults detection using layout data is presented. The detection of candidate fault portions embedded on the circuit is described. Two kinds of bridging faults are adjoining and crossed lines. These portions are easy to detect by layout data: DEF, LEF and Cell design data. For the selection of more reliable fault portions, the priority ranking is applied by using the size of the area that laps by expanding the line width (see Fig. 2).

3. Diagnosis concept

In this session, after a concept of the diagnosis procedure is presented, the detection way of impedance value being basic to this technology is described. One data for the way is transistor dimension, and other is its operating point. Next, the detection procedure is presented, and finally device for fault path tracing is introduced.

3.1. Diagnosis concept

The diagnosis technology being assist tool of physical analysis is requested with easy operation and short TAT. One of simple technologies is switching level simulation (SLS). SLS has been wildly used to evaluate the CMOS logic which treats each transistor as ON/OFF switching path. One of SLS applications is switching path modeling treated as stuck-at fault [3,4]. Voltage rather than stuck-at fault value is, however, beneficial data for precise fault diagnosis, and hence a novel way combined SLS with voltage analysis on transistor level has been developed.

The concept of this way is that transistor discerned as ON-switching path by SLS is replaced with impedance, and the circuit net composed of the transistors is replaced with impedance net,

* Tel.: +81 887 57 2118; fax: +81 887 57 2120.
E-mail address: sanada.masaru@kochi-tech.ac.jp

0026-2714/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2008.07.055

Author's personal copy

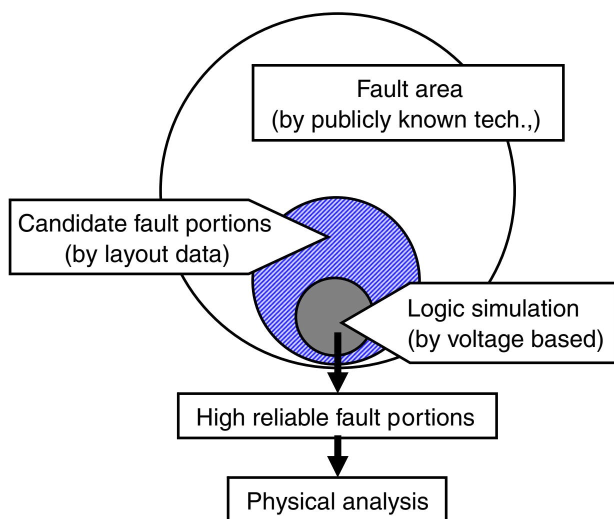


Fig. 1. Simplified diagnosis procedure.

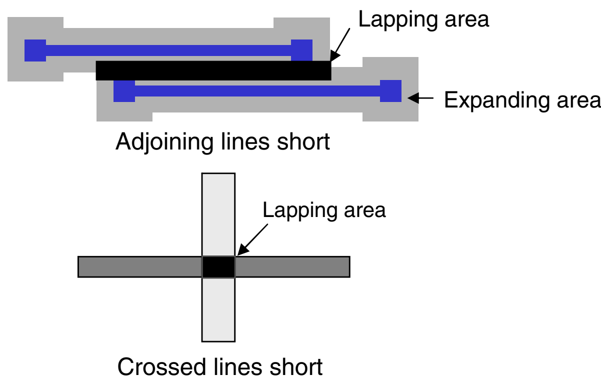


Fig. 2. Two kinds of candidate bridging faults.

following which voltage of each net node is computed by OHM's law. The impedance is calculated as the multiplication of the ratio of various transistor dimension to standard one and the ratio of the inverse of gradient value of various transistor operating point to one of normal operating point.

3.1.1. Transistor dimension

Transistor dimension formed with L (channel length) and W (channel width) is obtained by cell design data shown in Table 1. For the impedance detection of transistor with various dimension, the transistor composing Inverter gate is selected as standard transistor, and the ratio of L to W of the standard transistor is detected as normalized value. The impedance ratio of the various transistor is calculated as the ratio of L/W value to the normalized value.

3.1.2. Transistor operating point

The transistor operating point managed by gate voltage (V_G) affects impedance. When the power supply voltage (V_{DD}) is applied to the gate terminal, the operating point of N channel transistor (NchTr) and P channel transistor (PchTr) lies in non-saturation and cut-off area respectively, and the inverse of the gradient value between the NchTr's operating point and the origin ($\Delta V_{DS}/\Delta I_{DS}$) is assigned as NchTr's normal impedance value. When the ground (GND), the operating point of NchTr and PchTr lies in cut-off and non-saturation area respectively, and the inverse of the gradient value between the PchTr's operating point and the origin ($\Delta V_{DS}/\Delta I_{DS}$) is assigned as PchTr's normal impedance value. When the middle voltage out of V_{DD} or GND is applied to the gate terminal, the operating points of them are seated out of cut-off area and the impedance is several times larger than normal one.

The detection of the impedance is explained using Inverter gate. Fig. 3 shows the voltage transfer characteristics (VTC) of Inverter gate (see Fig. 3a) and the drain current (I_{DS}) versus drain voltage (V_{DS}) characteristics of NchTr and PchTr (see Fig. 3b), composing the Inverter gate. The coordinate system of PchTr is displayed according with NchTr. The area within $|dV_{OUT}/dV_{IN}| > 1$ decided by VTC curve is defined as middle domain (MD) with large impedance. When V_A, being input-voltage(V_{IN}) shown in Fig. 3a, is applied to INPUT terminal, PchTr operating point and NchTr are settled at point A shown in Fig. 3b. As a result, the PchTr's impedance/NchTr are calculated as the inverse of gradient value connecting point A and the origin($V_{DD}/0$) respectively, and the ratio of these values to the normal impedance value is computed.

For effective diagnosis, the table of impedance ratio of MD to normal domain is prepared on ahead. Fig. 4 shows the relation between VTC and impedance ratio, computed by Inverter gate designed with 0.35 μm rule. The area within 35% for V_{DD} to 65% is defined as MD. The impedance ratio in the MD is classified five steps (2 times, 3, 4, 5 and 6). The table shown in Fig. 4 denotes that PchTr/NchTr's impedance ratio in the range from 35% of V_{DD} to 42% are 2/6, 42% to 48% are 3/5, 48% to 52% are 4/4, 52% to 58% are 5/3, and 58% to 65% are 6/2 respectively.

At Appendix, an example of impedance calculation is introduced.

3.2. Detection procedure

An impedance detection procedure depending on bridge is shown in Fig. 5. The circuit with miss function by bridge brings generally penetration current net. First, transistor with the gate terminal connected to the fault line is treated as ON-state, and

Table 1
Cell design date

Transistor	Source	Gate	Drain	Base	Type	L	W
MN1	A000001	P01	R01	GND	NMOS	$L = 0.10\mu$	$W = 0.45\mu$
MN2	GND	R01	A000001	GND	NMOS	$L = 0.10\mu$	$W = 0.45\mu$
MP1	A000002	P02	R01	VDD	PMOS	$L = 0.10\mu$	$W = 0.72\mu$
MP2	VDD	R02	A000002	VDD	PMOS	$L = 0.10\mu$	$W = 0.72\mu$
MN3	A000003	P02	Q02	GND	NMOS	$L = 0.10\mu$	$W = 0.45\mu$
MN4	GND	Q01	A000003	GND	NMOS	$L = 0.10\mu$	$W = 0.45\mu$
MP3	A000004	P01	Q02	VDD	PMOS	$L = 0.10\mu$	$W = 0.72\mu$
MP4	VDD	Q01	A000004	VDD	PMOS	$L = 0.10\mu$	$W = 0.72\mu$
MN5	GND	Q01	A000007	GND	NMOS	$L = 0.10\mu$	$W = 1.20\mu$
MP5	VDD	Q01	A000007	VDD	PMOS	$L = 0.10\mu$	$W = 1.92u$

For example of impedance detection, MN3, MN5 and MP5 are used at Appendix.

Author's personal copy

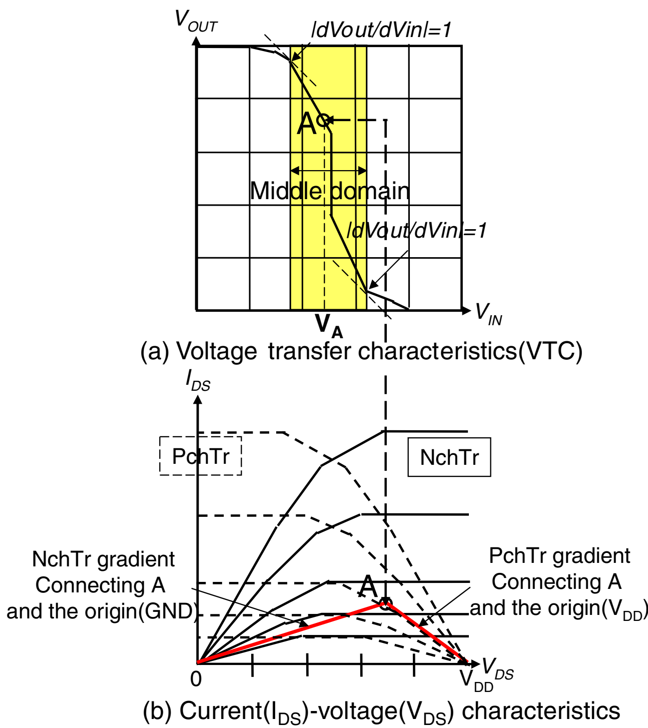


Fig. 3. VTC and $V_{DS} - I_{DS}$ curve of inverter gate.

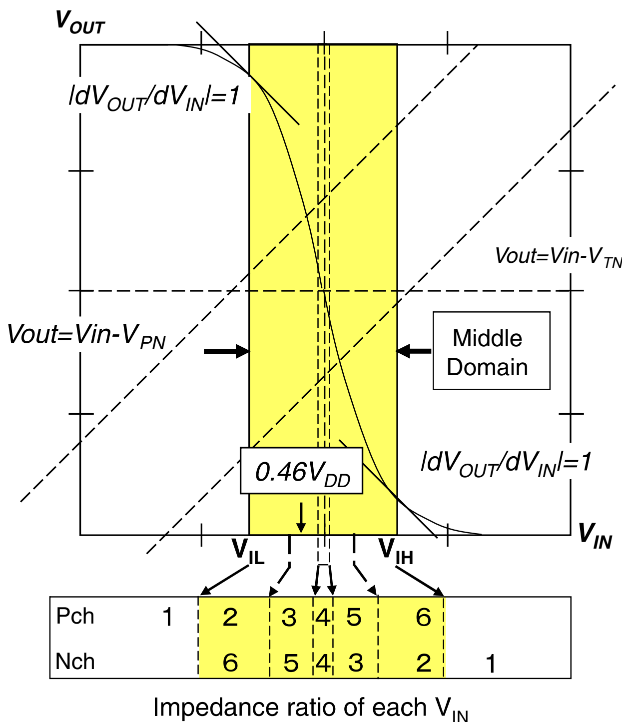


Fig. 4. Relation between VTC and impedance ratio table.

all transistors on the penetration current net are replaced with ON-switching path by SLS, following which impedance value is added to the transistors. At the addition of impedance, the simulation is repeated to draw out the optimized relation between gate voltage and impedance. Next, the switching path net is replaced with

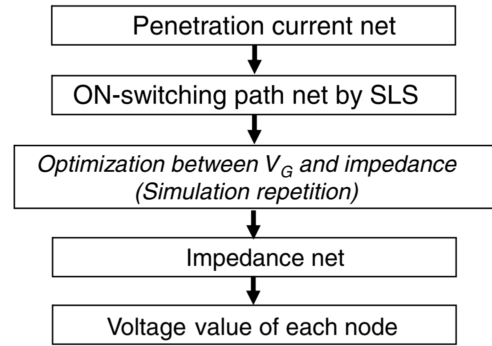


Fig. 5. Diagnosis procedure for bridge.

impedance net. After that, voltage of each node on the impedance net is computed by OHM's law.

3.2.1. Device for fault path tracing [5]

For fault path tracing, a virtual terminal (ViT) is prepared at output point which PchTr aggregate and NchTr one join. Each gate, composed of these transistors, is treated as one event unit of which operation time is defined as a normalized value "1", and hence the logic propagation time is obtained in the total number of event that the logic passes through.

4. Evaluation

In this session, the proposed diagnosis technology is evaluated. One is diagnosis precision by the comparison with SPICE, and other is fault path tracing bringing oscillation phenomenon.

4.1. Diagnosis precision compared with SPICE

Diagnosis accuracy was evaluated by using faulty full adder (FA) circuit with 3 inputs (A, B, C) and 2 outputs (COUT, SOUT). Table 2 shows logic table denoting normal logic and abnormal one. Abnormal logic in COUT was detected in 3 of 8 patterns which were combination with 3 input logic. SOUT was normal state. The 44 pieces of candidate fault patterns were detected by layout data, shown in Fig. 6. White rectangle/cycle patterns indicate candidate adjoining/crossed line portions. Note that line pairs between power supply voltage (V_{DD} or GND) and signal are not illustrated. Each candidate fault portions was embedded in the FA circuit. Relation between IN and OUT logic was detected by the simulation shown in the following procedure, and the fault portions were narrowed down, according with real fault logic. The diagnosis judged adjoining pair between Inverter (Inv) output line and 2-INPUT NAND (2inN) output line as fault portion. Fig. 7 shows FA circuit with the detected bridge fault. Fig. 7a indicates gate level circuit image and Fig. 7b

Table 2
Logic table of full adder circuit

A	B	C	COUT		SOUT	
			Normal output	Faulty sample	Normal output	Faulty sample
0	0	0	0	0	0	0
0	1	0	0	0	1	1
1	0	0	0	0	1	1
1	1	0	1	1	0	0
0	0	1	0	1	1	1
0	1	1	1	0	0	0
1	0	1	1	0	0	0
1	1	1	1	1	1	1
			Abnormal state		Normal state	

Author's personal copy

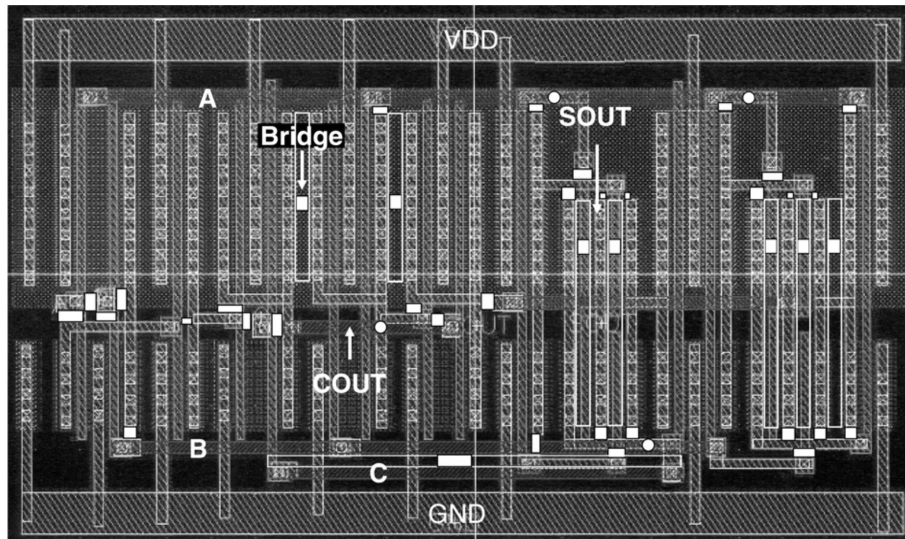


Fig. 6. Full adder circuit layout images.

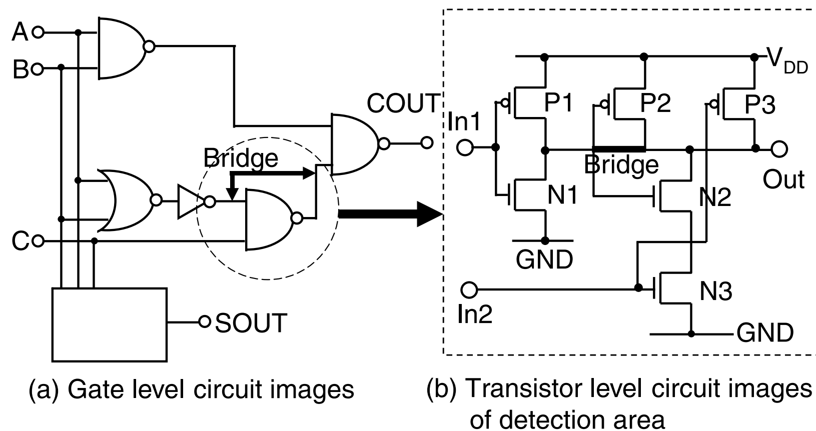


Fig. 7. Full adder circuit with bridge fault.

shows transistor level circuit of the detected fault area. The logic function of In1 and In2, being INPUT terminal, are indicated as NOT(A + B) and C, respectively.

When input-logic (1,1) is applied to input-terminal (In1,In2), normal circuit brings ON-state to N1, N3 and P2, and output (Out) does output "H" level. The circuit with the bridge, however, forms a penetration current net connecting from V_{DD} to GND through P2 and N1, and the voltage of the line connected to P2 and N2 gate terminal changes from GND to middle voltage out of V_{DD} or GND, following which a penetration current net pass through P2, N2 and N3 is newly formed. The transistors on the penetration current net are set down as ON-state, and the penetration current net is replaced with ON-switching path by SLS. These transistors on the path net are replaced with impedance net with optimized value by impedance detection way. After that voltage of each node on the net is computed by OHM's law, The OUTPUT(Out) voltage is detected as 0.23 V_{DD} according to Eq. (1). Note that n_{P2} and n_{N2} mean additional ratio for a standard value, and n_{P1}, n_{N1} and n_{N3} with normal V_G are approximately "1".

$$V_{OUT} = [\{1/(1+n_{N2})+1\}^{-1}/[\{1/(1+n_{N2})+1)\}^{-1}+n_{P2}]] \cdot V_{DD} \doteqdot \{1/(n_{P2}+1)\} \cdot V_{DD} = 0.23 \cdot V_{DD} \tag{1}$$

$$V_{OUT} = [(n_{N2}+1)/\{(1/1+1/n_{P2})^{-1}+(n_{N2}+1)\}] \cdot V_{DD} \doteqdot \{(n_{N2}+1)/(n_{N2}+2)\} \cdot V_{DD} = 0.82 \cdot V_{DD} \tag{2}$$

$$V_{OUT} = \frac{\{(n_{N4})^{-1}+(n_{N5})^{-1})\}^{-1}}{n_{P1}+\{(n_{N4})^{-1}+(n_{N5})^{-1})\}} \cdot V_{DD} = (1/3) \cdot V_{DD} \tag{3}$$

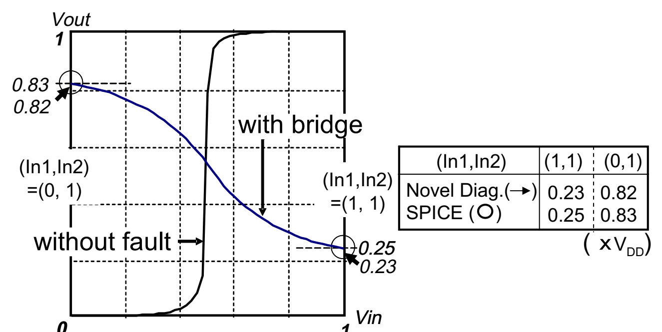


Fig. 8. Comparison of diagnosis result between this technology and SPICE.

Author's personal copy

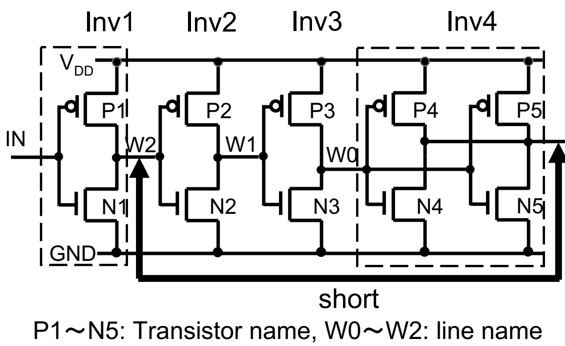


Fig. 9. Four steps sequential Inverter gate.

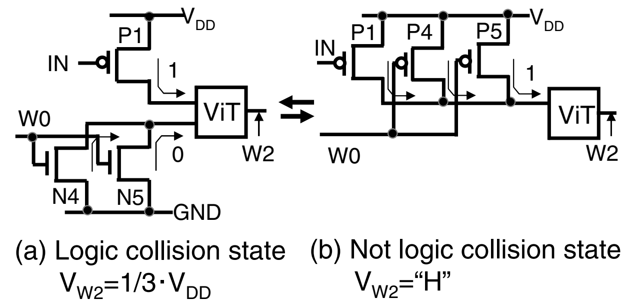


Fig. 10. Oscillation phenomenon.

When input-logic (0,1), the similar way to the above diagnosis detects output value with 0.82 V_{DD} (see Eq. (2)).

SPICE indicates that input-logic (1,1) outputs 0.25 V_{DD} and input-logic (0,1) outputs 0.83 V_{DD}. Both result denoted same output-voltage. Fig. 8 shows the characteristics of logic relation between V_{IN} (In1, In2) and V_{OUT} (Out), and the comparison of diagnosis accuracy between this technology and SPICE result with or without bridge. Operation time of this way was 1/100 times of SPICE by using SUN_ULTRA_60.

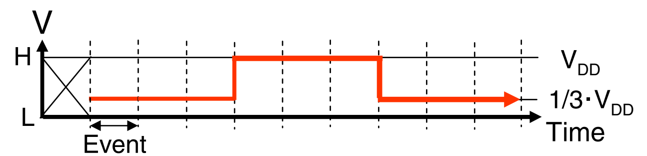


Fig. 11. Time chart with oscillation phenomenon.

4.2. Fault path tracing with oscillation phenomenon

Fault path tracing was evaluated by using simple circuit with four steps sequential Inverter gate (Inv1-Inv2-Inv3-Inv4) shown in Fig. 9. Inv4 is composed of parallel connection inverter gates and bridging fault is formed between Inv1 output line and Inv4 one. Note that all of the transistors composing Inverter gate are standard dimension type.

Logic collision

time	pin	value
0	VDD	1
0	VSS	0
0	IN	0
1	P1	1
1	P5	H
1	P4	H
1	P3	H
1	N1	Z
1	N5	L
1	N4	L
1	N3	L
1	N2	L
1	P2	H
2	W2	1
2	W1	0
2	W0	0
3	P2	Z
3	N2	0
3	P4	1
3	P5	1
3	N4	Z
3	N5	Z
3	P3	1
3	N3	Z

time	pin	value
4	W0	1
5	P4	Z
5	P5	Z
5	N4	0
5	N5	0
5	P1	1
5	N1	Z
6	W2	0
7	P2	1
7	N2	Z
8	W1	1
9	P3	Z
9	N3	0
10	W0	0
11	P4	1
11	P5	1
11	N4	Z
11	N5	Z
11	P1	1
11	N1	Z

time	pin	value
12	W2	1
13	P2	Z
13	N2	0
14	W1	0
15	P3	1
15	N3	Z
16	W0	1
17	P4	Z
17	P5	Z
17	N4	0
17	N5	0
17	P1	1
17	N1	Z
18	W2	0
19	P2	1
19	N2	Z
20	W1	1
21	P3	Z
21	N3	0

Initialization   Normal state

(P / N : PchTr / NchTr_drain terminal, W: Line name)

Fig. 12. Simulation result.

Author's personal copy

When "L" level is applied to Input (IN), "H" level is outputted at the Inv1 output terminal and "L" level is at Inv4, and the logic collision through the feedback loop between Inv1 output and Inv4 is generated, following which a penetration current net is brought by the logic collision phenomenon, and the net is treated as new event unit.

The logic collision which brings penetration current makes OFF-state of P4 and P5 and ON-state of P1, N4 & N5, and ON-switching path net is formed from V_{DD} to GND through P1, N4 and N5 by SLS (see Fig. 10a).

The ON-switching path net is replaced to impedance net, and voltage of each node is calculated, and hence the value of W2, being output terminal of the new event unit, is calculated as "$1/3 \cdot V_{DD}$" according in Eq. (3). Note that n_{P1}, n_{N4} and n_{N5} mean additional ratio for a standard value.

This value is judged as "L" because of outside of MD. The logic is propagated through Inv2 and Inv3, and "H" level is outputted at Inv4 terminal. Inv1 output logic is "H", and hence P1, P4 and P5 are ON-state, and N4 and N5 are OFF-state. This state does not bring logic collision and W2 value is kept to "H" level (see Fig. 10b). The above operation is repeated and the oscillation phenomenon is generated, shown in Fig. 11. The logic propagation time is obtained in the total number of event which logic passes through.

The simulation result of Input logic "L" is shown in Fig. 12. Time/pin/value, shown in Fig. 12, means event number/transistor drain or line name/logic value (1,0,H,L,Z) respectively. Time 1 to 3 shows logic initializing state. From time 4, diagnosis is started. At time 5 and 17, the logic collision is indicated, and at time 11 shows normal state. The oscillation phenomenon is repeated to each 3 event-times. Note that "W" being line name without operation time, does not be counted as event time.

By the similar diagnosis method, an oscillation phenomenon of the circuit applying input "H" is detected. In the oscillation, logic repeats between $2/3 \cdot V_{DD}$ and GND.

5. Conclusion

For fault path tracing, diagnosis technology combined with switching level simulation has been developed. The technology is the way to detect penetration current net result from fault, replace the net with impedance net, and calculate voltage value of each node of the impedance net. The segmentation of impedance value that was calculated by transistor operating point managed by gate voltage improved the fault diagnosis precision. The virtual terminal (ViT), that was prepared at output point which PchTr aggregate and NchTr one join, made it possible to trace the fault path propagation. The comparison of this way with SPICE indicated an approximately same diagnosis result. Operation time of this way was 1/100 times of SPICE using SUN_ULTRA_60. The detected doubtful portions are quickly applied to physical analysis.

Acknowledgement

I would like to thank the design crew at ASTRON Corp. in Japan for discussion and software development.

Appendix

An example of impedance detection is presented using cell design data shown in Table 1. MN5 (NchTr) with $L/W = 0.1\mu/1.20\mu$ and MP5 (PchTr) with $L/W = 0.1\mu/1.92\mu$ composing Inverter gate are selected as standard transistor. Considering MN3 (NchTr) with $L/W = 0.1\mu/0.45\mu$, the L/W value ratio of MN3 to standard transistor MN5 is calculated as 2.67 (see Eq. (4)).

$$\mathrm{MN3}(L/W = 0.1\mu/0.45\mu) \div \mathrm{MN5}(L/W = 0.1\mu/1.20\mu) = 2.67 \tag{4}$$

When $0.46\,V_{DD}$ voltage is applied to MN3 gate terminal (VIN = NchTr's VG), the impedance ratio of the MN3 operating domain to normal operating domain is detected as 5 times (see Fig. 4). The impedance is, as a result, calculated as 13.33, being the multiplication of the ratio of L/W value and the ratio of impedance value led by operating point (see Eq. (5)).

$$2.67 \times \text{additional ratio}(5) = 13.33 \tag{5}$$

.

References

[1] Sanada M, Yoshizawa Y. Fault diagnosis technology based on transistor behavior analysis. Microelectron Reliab 2006;46(9–11):1575–80.
[2] Sato Y, Sugiura K, Shimoda R, Yoshizawa Y, Norimatsu K, Sanada M. Defect diagnosis – reasoning methodology. ATS2006. p. 209–41.
[3] Krishnaswamy V, Casas J, Tezlaff T. A switch level fault simulation environment. ACM-DAC2000. p. 780–85.
[4] Amyeen ME, Nayak D, Venkataraman S. Improving precision using mixed-level fault diagnosis. ITC2006. p. 22.3.
[5] Sanada M, Nakamura T, Hashida K. Fault path tracing based on transistor operating point – detection of oscillation phenomenon by feedback fault. LTS2007. p. 251–56 [Japanese edition].